Versatile Power Supply Tracking without MOSFETs

by Dan Eddleman

Introduction

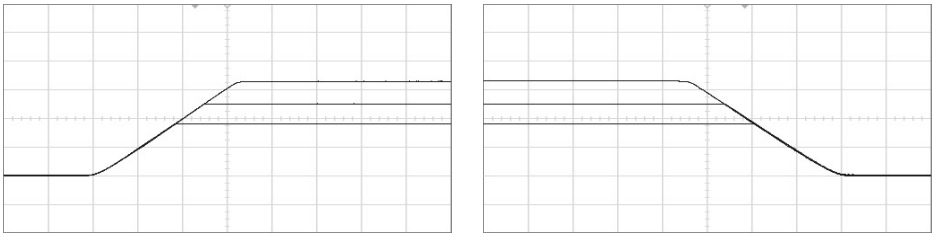
Modern electronics systems often have complex power supply voltage tracking and sequencing requirements. Ignoring these requirements can result in the immediate destruction of devices, or worse yet, premature failures in the field.

Voltage tracking requirements usually specify that the voltage difference between two power supplies must never exceed a certain limit. This constraint applies at all times: during power up, power down, and steady state operation.

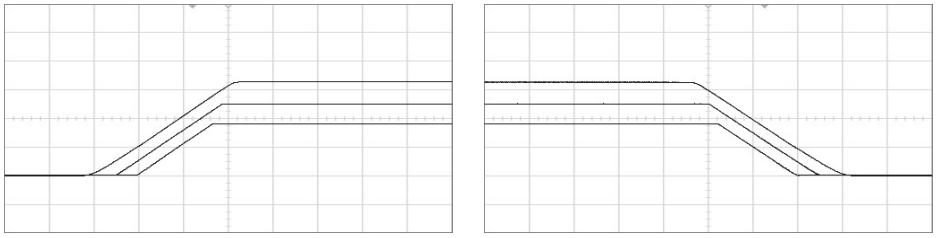
In contrast, *supply sequencing* requirements specify the order in which supplies power up and power down.

Figure 1 shows various tracking and sequencing scenarios.

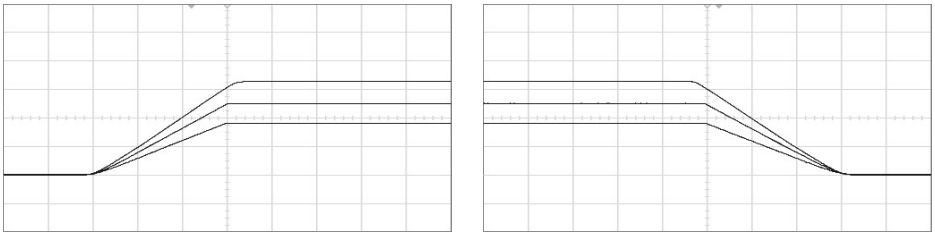
The penalty for poor tracking or sequencing is often irreparable damage to devices in the system. FGPAs, PLDs, DSPs and microprocessors typically have diodes placed between the core and I/O supplies as a component of the ESD protection. If the supplies violate the tracking requirements and forward bias the protection diodes, the device may be damaged.



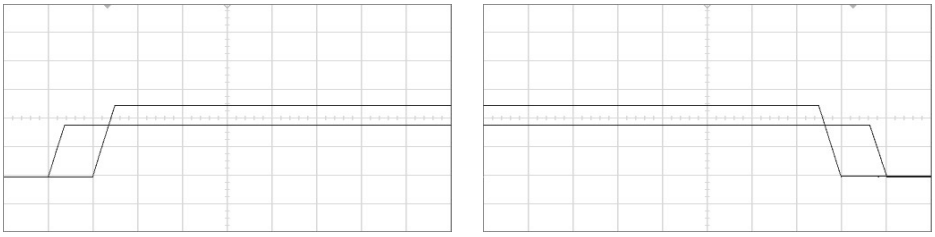
a. Coincident tracking



b. Offset tracking



c. Ratiometric tracking



d. Supply sequencing

Figure 1. Types of power supply voltage tracking

Forward biasing internal diodes, whether protection diodes or other diodes inherent to the CMOS process, may trigger latchup destroying the device. In other cases, when the I/O supply rises before the core supply, undefined logic states in the core can cause excessive current in the I/O circuitry. Even when the individual components of a system do not require supply tracking or sequencing, the complete system may require power supply sequencing for proper operation. For example, a system clock may need to start before a block of logic is powered.

A Simple and Versatile Solution

The LTC2923 provides a simple and versatile solution to both power supply tracking and sequencing without the drawbacks of series MOSFETs.

By selecting a few resistors, the supplies are configured to ramp-up and ramp-down with a variety of voltage profiles. Tracking requirements can dictate that supply voltages are equal during ramp up and ramp down (Figure 1a), or that the supplies must ramp up and down with fixed voltage offsets between them (Figure 1b), or that they must ramp up and down ratiometrically (Figure 1c). Alternatively, supply sequencing may be required, which can also be handled by the LTC2923 (Figure 1d).

Many voltage tracking solutions use series MOSFETs, which have the problems of an inherent voltage drop, additional power consumption, and extra PC board real estate.

Instead, the LTC2923 controls supplies by injecting current into their feedback nodes and thus avoids the pass element losses inherent in series MOSFET solutions. Furthermore, power supply stability and transient response remain unaffected because the injected current from the LTC2923 offsets the output voltage without al-

tering the power supply control loop dynamics.

Power supply tracking is straightforward with the LTC2923. It controls two slave supplies that track a master signal. A pair of resistors configures the behavior of each slave supply relative to the master signal. The choice of resistors can cause a slave supply to track the master signal exactly or with a different ramp rate, voltage offset, time delay, or combination of these.

An optional series FET provides support for a third supply or any supply that does not allow direct access to its feedback resistors, such as module power supplies, as shown in Figure 2. When the optional series FET is used, its output serves as the master signal. If the series FET is not used, the master signal is generated by tying a capacitor from the GATE and RAMP pins to ground as shown in Figure 3.

How a Simple Cell Tracks and Sequences Supplies

The operation of the LTC2923 is based on the simple tracking cell shown in Figure 4. This cell servos the TRACK pin to 0.8V and mirrors the current supplied by that pin at the FB pin. Connecting a resistive divider from the master signal to the TRACK pin configures the FB pin's current as a function of the master signal. By selecting the appropriate resistor values, R_{TA} and R_{TB}, it is possible to generate any of the profiles shown in Figure 1.

The LTC2923's data sheet outlines a simple 3-step procedure to choose resistor values for each of the supply behaviors shown in Figure 1. This procedure is described in the data sheet and reprinted in the sidebar here. The rest of this section covers a more in-depth analysis of the operation of the LTC2923.

Examine the schematic shown in Figure 5, and assume that the DC/DC converter's feedback voltage is 0.8V.

Now, consider the case where V_{MASTER} = 0V. Here, the current from the TRACK pin flows through R_{TA} and R_{TB}, which are both grounded. The tracking cell mirrors this same current at the FB pin. Because $R_{TA} = R_{FA}$ and $R_{TB} = R_{FB}$, 0.8V is forced at the feedback node of the DC/DC converter. This

Tracking and/or Sequencing Power Supplies is as Easy as 1, 2, 3

Any of the profiles shown in Figure 1 can be achieved by using the following simple design procedure. Figure 2 shows a basic three-supply application circuit.

1. *Set the ramp rate of the master signal.*

   Solve for the value of C_{GATE}, the capacitor on the GATE pin, based on the desired ramp rate (V/s) of the master supply, S_M.

   $$C_{GATE} = \frac{I_{GATE}}{S_M} \text{ where } I_{GATE} \approx 10\mu A \quad (1)$$

   If the external FET has a gate capacitance comparable to C_{GATE}, then the external capacitor's value should be reduced to compensate for the FET's gate capacitance.

   If no external FET is used, tie the GATE and RAMP pins together.

2. *Solve for the pair of resistors that provide the desired ramp rate of the slave supply, assuming no delay.*

   Choose a ramp rate for the slave supply, S_S. If the slave supply ramps up coincident with the master supply or with a fixed voltage offset, then the ramp rate equals the master supply's ramp rate. Be sure to use a fast enough ramp rate for the slave supply so that it will finish ramping before the master supply has reached its final supply value. If not, the slave supply will be held below the intended regulation value by the master supply. Use the following formulas to determine the resistor values for the desired ramp rate, where R_{FB} and R_{FA} are the feedback resistors in the slave supply and V_{FB} is the feedback reference voltage of the slave supply:

   $$R_{TB} = R_{FB} \bullet \frac{S_M}{S_S} \quad (2)$$

   $$R_{TA}' = \frac{V_{TRACK}}{\frac{V_{FB}}{R_{FB}} + \frac{V_{FB}}{R_{FA}} - \frac{V_{TRACK}}{R_{TB}}} \quad (3)$$

   where $V_{TRACK} \approx 0.8V$.

   Note that large ratios of slave ramp rate to master ramp rate, S_S/S_M, may result in negative values for R_{TA}'. If a sufficiently large delay is used in step 3, R_{TA} will be positive, otherwise S_S/S_M must be reduced.

3. *Choose R_{TA} to obtain the desired delay.*

   If no delay is required, such as in coincident and ratiometric tracking, then simply set $R_{TA} = R_{TA}'$. If a delay is desired, as in offset tracking and supply sequencing, calculate R_{TA}'' to determine the value of R_{TA} where t_D is the desired delay in seconds.

   $$R_{TA}'' = \frac{V_{TRACK} \bullet R_{TB}}{t_D \bullet S_M} \quad (4)$$

   $$R_{TA} = R_{TA}' \,||\, R_{TA}'' \quad (5)$$

   the parallel combination of R_{TA}' and R_{TA}''

   As noted in step 2, small delays and large ratios of slave ramp rate to master ramp rate (usually only seen in sequencing) may result in solutions with negative values for R_{TA}. In such cases, either the delay must be increased or the ratio of slave ramp rate to master ramp rate must be reduced.

results in an output voltage, V_{SLAVE}, of 0V. Any voltage greater than 0V at the DC/DC converter's output results in a feedback voltage greater than 0.8V causing the converter to drive its output towards 0V. So, with $R_{TA} = R_{FA}$ and $R_{TB} = R_{FB}$, $V_{SLAVE} = 0V$ when $V_{MASTER} = 0V$.

Now, consider the case in Figure 6 where $V_{MASTER} = 2.5V$, the nominal output voltage of the DC/DC converter. Without the LTC2923, the DC/DC converter's feedback network drives 0.8V at its feedback node while generating an output voltage of 2.5V. Since $R_{TA} = R_{FA}$ and $R_{TB} = R_{FB}$, the resistive divider formed by R_{TA} and R_{TB} forces 0.8V at the TRACK pin when $V_{MASTER} = 2.5V$, without requiring any current from the tracking cell. Since the tracking cell only sources current, no current flows from the TRACK pin when $V_{MASTER} \geq 2.5V$. Therefore, when V_{MASTER} is above 2.5V the DC/DC converter operates as if the tracking cell were not present.

The relationship between V_{MASTER} and V_{SLAVE} is linear between 0V and 2.5V, so the fact that the DC/DC converter's output is equal to V_{MASTER} at 0V and at 2.5V means that V_{MASTER} and V_{SLAVE} are equal at all points in between. The DC/DC converter's output tracks V_{MASTER} exactly until V_{MASTER} rises above 2.5V. When V_{MASTER} is above 2.5V, no current flows from the FB pin and the tracking cell is effectively removed from the circuit.

The fact that $R_{TA} = R_{FA}$ and $R_{TB} = R_{FB}$ in this example is not just a fortunate coincidence. For a DC/DC converter with a feedback voltage of 0.8V, setting the track resistors, R_{TA} and R_{TB}, equal to the feedback resistors, R_{FA} and R_{FB} causes the supplies to track together exactly. When the feedback voltage is not equal to 0.8V, only R_{TA} needs to be adjusted, a result that is discussed below.

R_{TB} Configures the Ramp Rate

The LTC2923 really shows flexibility when $R_{TA} \neq R_{FA}$ and/or $R_{TB} \neq R_{FB}$. First consider the effects of R_{TB}'s value.

R_{TB} configures the ramp rate of the slave supply. More accurately, R_{TB} configures the gain of the slave supply relative to the master supply and ultimately determines the ramp rate. Continuing with the example in Figure 5, as long as the track cell is regulating the TRACK pin at 0.8V (which is true for $V_{MASTER} < 2.5V$), the current through R_{TA} is fixed at 0.8/R_{TA}. Therefore, the current change in response to a voltage change at V_{MASTER} is completely determined by R_{TB}, as shown in Figure 7. Because one end

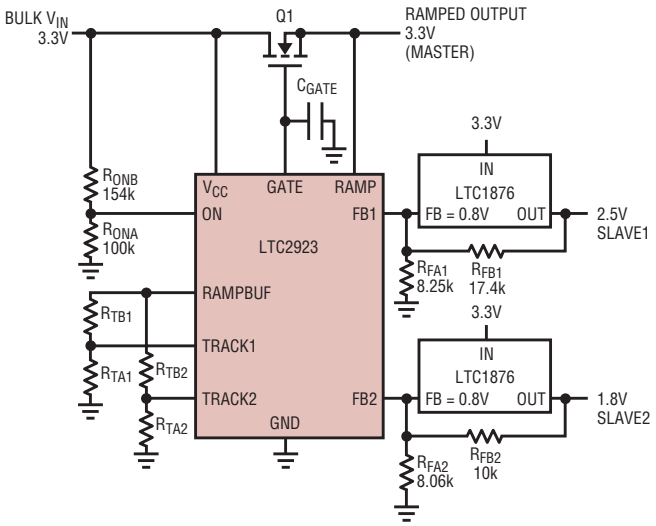


Figure 2. Typical coincident tracking application. The optional series FET is used to ramp the 3.3V bulk supply.

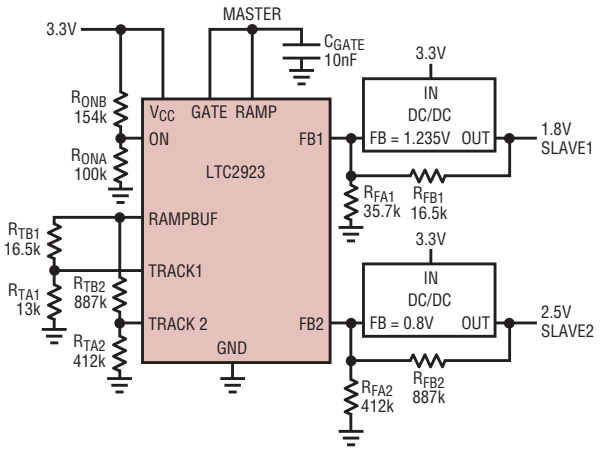


Figure 3. If the series FET is not used, the master signal is generated by tying a capacitor from the GATE and RAMP pins to ground.

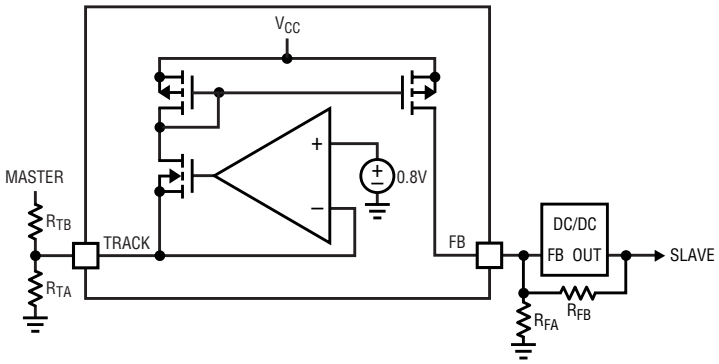


Figure 4. Simplified tracking cell

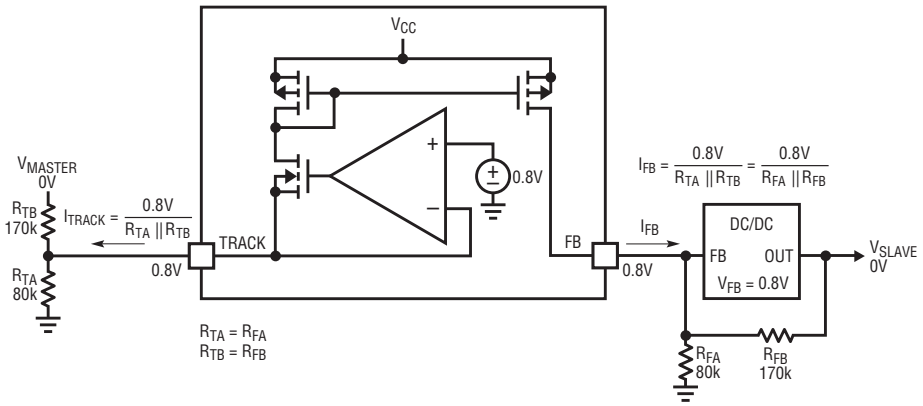


Figure 5. I_{FB} forces V_{SLAVE} to 0V

of the resistor R_{TB} is fixed at 0.8V, the change in current from the TRACK pin is equal to

$$\Delta I_{TRACK} = \frac{\Delta V_{MASTER}}{R_{TB}} \quad (6)$$

This change in current is mirrored at the FB pin. Since the DC/DC converter regulates its feedback node to 0.8V, the voltage across R_{FA} is fixed at 0.8V, and thus the current through R_{FA} is also fixed. Any change in the current from the FB pin results in an equal change in the current across R_{FB}. If $R_{TB} = R_{FB}$ then any change in voltage at V_{MASTER} results in an equal change in the voltage at the DC/DC converter's output, V_{SLAVE}. If R_{FB} is increased relative to R_{TB} the voltage change at V_{SLAVE} is greater than the voltage change at V_{MASTER}. The change in voltage at the DC/DC converter's output is:

$$\Delta I_{FB} \bullet R_{FB} = \Delta I_{TRACK} \bullet R_{FB} \quad (7)$$

$$\Delta V_{SLAVE} = \frac{\Delta V_{MASTER}}{R_{TB}} \bullet R_{FB}$$

$$= \Delta V_{MASTER} \bullet \frac{R_{FB}}{R_{TB}}$$

This can be interpreted as a gain of R_{FB}/R_{TB} between the master signal and the output voltage.

Because an external capacitor connected to the GATE pin programs the master supply's ramp rate at:

$$\frac{\Delta V_{MASTER}}{\Delta t} = \frac{10\mu A}{C_{GATE}}, \quad (8)$$

the ramp rate of the slave supply is:

$$\frac{\Delta V_{SLAVE}}{\Delta t} = \frac{10\mu A}{C_{GATE}} \bullet \frac{R_{FB}}{R_{TB}}. \quad (9)$$

R_{TA} Corrects for Converter V_{REF}

As mentioned above, R_{TA} is adjusted when a DC/DC converter's feedback voltage is not equal to 0.8V. If, for example, the DC/DC converter's feedback voltage is 1.2V, then the current from the FB pin, I_{FB}, needed to hold the converter's output at 0V is

$$I_{FB} = \frac{1.2V}{R_{FA} \,||\, R_{FB}} \quad (10)$$

$R_{TB} = R_{FB}$ still sets the gain between V_{MASTER} and V_{TRACK} to 1V/V. If V_{MASTER} is at 0V, then I_{TRACK} just barely holds V_{SLAVE} at 0V when

$$I_{TRACK} = I_{FB} \quad (11)$$

$$\frac{0.8V}{R_{TA} \,||\, R_{FB}} = \frac{0.8V}{R_{FA} \,||\, R_{FB}}$$

Solving for R_{TA} gives the exact value of R_{TA} that compensates for the 1.2V feedback voltage as opposed to the 0.8V value.

This value of R_{TA}, the value that sets V_{SLAVE} to track V_{MASTER} with no delay, is represented by R_{TA}' in the 3-step design procedure.

R_{TA} Configures an Offset

R_{TA} not only compensates for the DC/DC converter's feedback voltage, it serves an even broader purpose. It configures an offset voltage between V_{MASTER} and V_{SLAVE}.

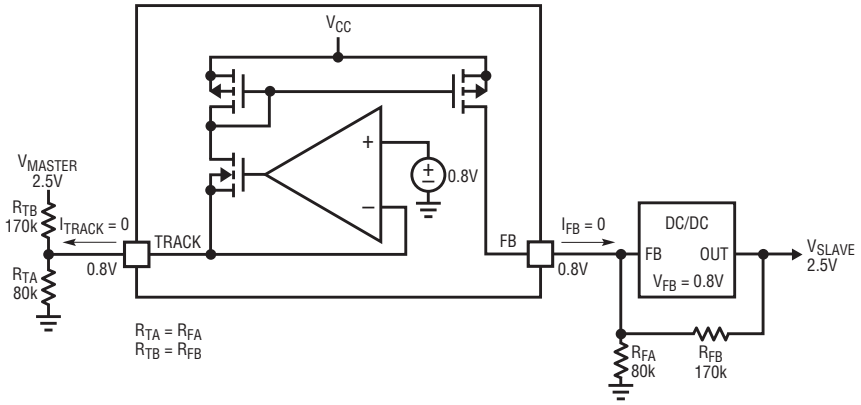


Figure 6. V_{SLAVE} = 2.5V when V_{MASTER} = 2.5V

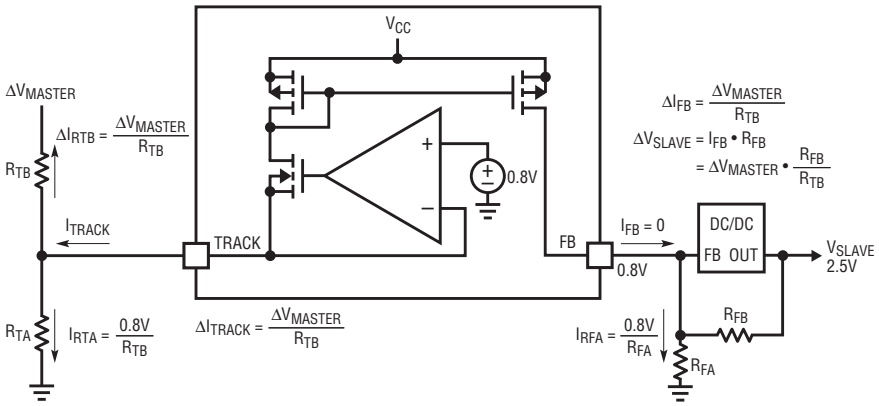


Figure 7. R_{TB} configures gain (ramp rate)

To demonstrate this, assume that R_{TA} is reduced to 62kΩ so that $R_{TA} < R_{FA}$ as shown in Figure 8. This creates the voltage profile shown in Figure 9. Compared to the previous example, more current flows from the TRACK pin when V_{MASTER} is at ground. The output of the DC/DC converter remains at ground until V_{MASTER} rises high enough to reduce the current from the TRACK pin to the level that just holds V_{SLAVE} at 0V:

$$I_{TRACK} = I_{FB} = \frac{0.8V}{R_{FA} \,||\, R_{FB}} \qquad (12)$$

$$\frac{0.8V}{R_{TA}} - \frac{\Delta V_{MASTER} - 0.8V}{R_{TB}} = \frac{0.8V}{R_{FA} \,||\, R_{FB}}$$

$$\frac{0.8V}{62k\Omega} - \frac{\Delta V_{MASTER} - 0.8V}{170k\Omega} = \frac{0.8V}{80k\Omega \,||\, 170k\Omega}$$

$$\Delta V_{MASTER} = 0.5V$$

The gain between V_{SLAVE} and V_{MASTER} is still determined by R_{FB}/R_{TB} as V_{SLAVE} ramps from 0V to 2.5V, and the voltage across R_{TA} is still 0.8V, so the ramp rate does not vary with R_{TA}. V_{SLAVE}, however, does not rise above 0V until V_{MASTER} reaches 0.5V in this example.

In the 3-step design procedure, the slave supply is offset by R_{TA}'', the value of resistor that is placed in parallel with R_{TA}' to produce the desired offset.

R_{TA} Configures a Delay

Alternatively, the voltage offset generated by R_{TA} may be interpreted as a time delay between the supplies. In the above example it was shown that V_{SLAVE} remains at ground until V_{MASTER} rises above 0.5V. Since the ramp-rate is 1000V/s and V_{SLAVE} follows 0.5V below V_{MASTER}, this can also be interpreted as a time delay of

$$T_D = \frac{0.5V}{1000V/s} = 0.5ms$$

This representation is helpful when implementing supply sequencing. To sequence supplies, the slave supplies are ramped up at a faster rate than the master signal and each is delayed.

By choosing the appropriate ramp rates and time delays, each supply is completely powered before the next supply ramps up. Multiple iterations may be necessary to find an acceptable solution since small delays combined with large slave ramp rate to master ramp rate ratios may result in negative values for R_{TA}. Also, the chosen values for R_{TA} and R_{TB} must not require more than 1mA from the TRACK pin.

In the 3-step design procedure this delay is achieved with R_{TA}'', the value of resistor that is placed in parallel with R_{TA}' to produce the desired delay.

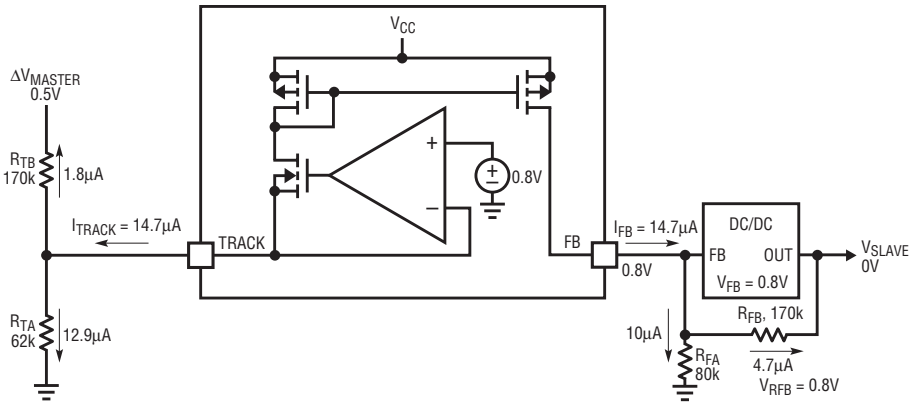


Figure 8. $R_{TA} < R_{FA}$ configures offset tracking

Examples

Now consider how varying R_{TA} and R_{TB} can produce each of the voltage tracking profiles in Figure 1. The schematic in Figure 2 uses an LTC1876 dual synchronous step-down converter to produce 2.5V and 1.8V supplies from a 3.3V input. An LTC2923 connected to the feedback nodes controls the ramp-up and ramp-down behavior of these supplies. In the following example, the 3-step design procedure outlined in the sidebar is followed.

An external Si2306 MOSFET controls the behavior of the 3.3V supply with the ramp-rate determined by the capacitor on the GATE pin. Following Step 1 of the 3-Step design procedure, if a ramp-rate, S_M, of 1000V/s is desired, equation (1) results in:

$$C_{GATE} = 10nF$$

If ramp-rate accuracy is critical then the external MOSFET's gate capacitance should be subtracted from the C_{GATE} capacitor's value. If no MOSFET is used, tie the GATE and RAMP pins together and connect the C_{GATE} capacitor between those pins and ground.

Coincident Tracking

Consider coincident tracking as shown in Figure 1a. We know from the above discussion that if the feedback voltage of the switching power supply is 0.8V, as it is on the LTC1876, then coincident tracking can be configured by setting the tracking resistors equal to the feedback resistors. In this case,

$$R_{TA1} = R_{FA1}$$
$$R_{TB1} = R_{FB1}$$
$$R_{TA2} = R_{FA2}$$
$$R_{TB2} = R_{FB2}$$

Verify this conclusion by following Step 2 of the 3-Step Design Procedure. From equation (2):

$$R_{TB1} = 17.4k\Omega$$
$$R_{TB2} = 10k\Omega$$

And from equation (3):

$$R_{TA1}' = 8.25k\Omega$$
$$R_{TA2}' = 8.06k\Omega$$

As mentioned above, in the 3-step design procedure R_{TA}' represents the value of R_{TA} that produces no delay or offset. Since no delay is desired, $R_{TA1} = R_{TA1}'$ and $R_{TA2} = R_{TA2}'$, and Step 3 of the Design Procedure is unnecessary.

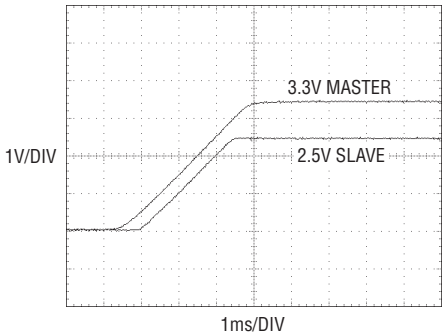


Figure 9. Output profile of circuit in Figure 8

Ratiometric Tracking

Now consider ratiometric tracking as seen in Figure 1b. Set the slave ramp-rates, S_{S1} and S_{S2}:

$$S_{S1} = 1000\,V/s \bullet \frac{2.5V}{3.3V} \quad (13)$$

$$= 758V/s$$

$$\approx 800V/s$$

$$S_{S2} = 1000\,V/s \bullet \frac{1.8V}{3.3V} \quad (14)$$

$$= 545V/s$$

$$\approx 600V/s$$

Round up the ramp-rates, S_{S1} and S_{S2}, to 800V/s and 600V/s so that there is no chance of the 3.3V supply voltage holding the 2.5V or 1.8V supplies low after the ramp-up is complete.

Solving equation (3) from Step 2 of the Design Procedure:

$R_{TB1} \approx 21.5k\Omega$
$R_{TB2} \approx 16.9k\Omega$

This agrees with the intuitive expectation that R_{TB1} and R_{TB2} should be less than R_{FB1} and R_{FB2}, because we desire gains of less than 1V/V between the master and the slave supplies. (Remember that the gain is R_{FB}/R_{TB}.)

To complete Step 2, we must also solve for R_{TA1}' and R_{TA2}' using equation (3).

$R_{TA1}' \approx 7.5k\Omega$
$R_{TA2}' \approx 6.04k\Omega$

Since no delay is desired, $R_{TA1} = R_{TA1}'$ and $R_{TA2} = R_{TA2}'$ and Step 3 is unnecessary.

Offset Tracking

In this example, the 2.5V supply ramps up 0.5V below the 3.3V supply, and the 1.8V supply ramps up 1V below the 3.3V supply, as shown in Figure 1c. In offset tracking, the ramp-rates are equal so the gain between the master and slave supplies is 1V/V. As in Step 1 of the coincident tracking example:

$R_{TB1} = R_{FB1} = 17.4k\Omega$
$R_{TB2} = R_{FB2} = 10k\Omega$

Remember that R_{TA} is used to configure the offsets. We know intuitively that R_{TA1} and R_{TA2} should be smaller than in the coincident tracking example to generate offsets in the slave outputs. We already found that

$R_{TA1}' = R_{FA1} = 8.25k\Omega$
$R_{TA2}' = R_{FA2} = 8.06k\Omega$

in the coincident tracking example above. Now we can use Step 3 of the Design Procedure to solve for R_{TA1} and R_{TA2} after converting the voltage offset to a time delay.

$$t_{D1} = \frac{V_{OS1}}{S_{S1}} \quad (15)$$

$$= 0.5V/1000(V/s)$$

$$= 0.5ms$$

$$t_{D2} = \frac{V_{OS2}}{S_{S2}} \quad (16)$$

$$= 1V/1000(V/s)$$

$$= 1ms$$

From equation (4):

$R_{TA1}'' = 27.8k\Omega$
$R_{TA2}'' = 8k\Omega$

Remember that R_{TA}'' is the value of resistor that is placed in parallel with R_{TA}' to produce the desired offset. Therefore, R_{TA1} and R_{TA2} can be found from equation (5):

$R_{TA1} \approx 6.34k\Omega$
$R_{TA2} \approx 4.02k\Omega$

Supply Sequencing

To produce a voltage profile such as the one shown in Figure 1d, supply sequencing applications require the slaves to have fast ramp rates and time delays relative to the master. First, reducing the master signal ramp-rate to 100V/s using the equation from Step 1 of the Design Procedure results in:

$C_{GATE} = 100nF$

Set the slave ramp rates to 500V/s in equation (2) to find R_{TB1} and R_{TB2}:

$R_{TB1} = 3.48k\Omega$
$R_{TB2} = 2k\Omega$

Intuitively, R_{FB}/R_{TB} should be 5 times greater than the previous examples since the gain from the master signal to the slave supply is now 5 times greater.

Complete Step 2 by solving for R_{TA1}' and R_{TA2}' using equation (3).

$R_{TA1}' = -9.20k\Omega$
$R_{TA2}' = -3.62k\Omega$

Step 3 adjusts R_{TA1} and R_{TA2} for the desired delays between the two supplies. In this case, factor in a delay of 20ms for the 2.5V supply relative to the master signal and a delay of 10ms for the 1.8V supply.

$R_{TA1}'' = 1.39k\Omega$

$R_{TA1} = R_{TA1}' || R_{TA1}''$

$\approx 1.65k\Omega$

$R_{TA2}'' = 1.6k\Omega$

$R_{TA2} = R_{TA2}' || R_{TA2}''$

$\approx 2.87k\Omega$

Note that not every combination of ramp-rates and delays is possible. Small delays and large ratios of slave ramp rate to master ramp rate may result in solutions that require negative resistors. In such cases, either the delay must be increased or the ratio of slave ramp rate to the master ramp rate must be reduced. In addition, the chosen resistor values should not require more than 1mA to flow from the TRACK and FB pins. Therefore, confirm that less than 1mA flows from TRACK when V_{MASTER} is at 0V.

$$I_{TRACK1} = \frac{V_{TRACK}}{R_{TA1} || R_{TB1}} \quad (17)$$

$$= 0.718mA < 1mA$$

$$I_{TRACK2} = \frac{V_{TRACK}}{R_{TA2} || R_{TB2}} \quad (18)$$

$$= 0.679mA < 1mA$$

Conclusion

The LTC2923 simplifies power supply tracking and sequencing while offering superior performance in a smaller area than competing solutions. A few resistors can configure simple or complex supply behaviors. In most cases, series MOSFETs are eliminated along with their parasitic voltage drops and power consumption, but for those designs that require a series MOSFET, support is provided for one. The LTC2923 offers all of these features in a tiny MS10 or leadless 12-pin DFN package.